SDR Structure Based CFO Estimation and Compensation Circuit for OFDM Systems Using Reconfigurable CORDIC FPGA Modules

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***tract*—In this paper, a software defined radio (SDR) ucture based carrier frequency offset (CFO) estimation and pensation circuit is designed for an orthogonal frequency ision multiplexing (OFDM) system using the reconfigurable rdinate rotation digital computer (CORDIC) field grammable gate array (FPGA) rotation and vectoring uit modules. The SDR architecture of the CFO estimation compensation circuit and the program flow of the CORDIC GA modules are presented. The required processing time hardware reconfiguration function are our major design siderations. The experimental results demonstrate that the igned CFO estimation and compensation circuit plemented with a 10 MHz clock FPGA chip can reduce the idual CFO to an acceptable range within 1.5μsec.**

I. INTRODUCTION

Carrier frequency offset (CFO) occurs, if the frequency is smatched in the transmitter and the receiver oscillators or Doppler frequency exists between the transmitter and eiver. For an orthogonal frequency division multiplexing DM) system, the CFO can result in inter-subcarrier erference (ICI). In order to suppress the ICI and thereby ce signal to noise ratio (SNR) degradation, the residual must be sufficiently small. In [1], analytic results show when using the 64-QAM constellation, it is better to the residual CFO below 0.01 subcarrier spacing to re the SNR degradation is less than 0.3 dB. When the SK is used, the residual CFO can be up to 0.03 subcarrier cing.

he trend of future multimedia broadband communication tems is the utilization of modularized FPGA chips [2] in ware defined radio (SDR), which accepts commands for erent operating modes. By varying the parameters in the ne hardware modules, the SDR can quickly allocate nerous different purposed modules to efficiently realize icular algorithms involving repetitive and intensive culations [3]. On the other hand, many of the wireless munications algorithms require the evaluation of mentary functions, such as trigonometric and phase angle ration functions, which cannot be supported by FPGA delSim's library [4]. To efficiently evaluate each of these mentary functions also motivated the development of the rdinate rotation digital computer (CORDIC) [5] modules, ich offers a unified iterative formulation to efficiently luate each of these elementary functions. By varying a simple parameters, the same CORDIC processor is able of iteratively evaluating these elementary functions ng the same hardware within the same amount of time. In study, the CORDIC rotation and vectoring modules are realized in the FPGA in order to implement the CFO estimation and compensation circuits of an OFDM system based on SDR architecture. Finally, the 64-QAM training symbols are used to test the required processing time and accuracy of the CFO estimation and compensation circuits.

II. PRINCIPLES

With reference to the conventional channel estimation approach of a given OFDM system [6], ten short OFDM training signals are used for packet detection, coarse frequency offset estimation and timing synchronization. If s_n is the short training symbol, then the discrete transmit signal is

$$y_n = s_n \exp(j2\pi f_{tx} n T_s) \tag{1}$$

, where f_{tx} is the transmit carrier frequency and T_s is the sampling interval. The discrete received baseband training symbol is

$$r_n = s_n \exp(j2\pi f_\Delta n T_s) \tag{2}$$

, where the CFO $f_\Delta = f_{tx} - f_{rx}$ and f_{rx} is the receive carrier frequency. The autocorrelation function of r_n is derived as

$$\begin{aligned} z &= \sum_{n=0}^{D-1} r_n r_{n+D}^* \\ &= \sum_{n=0}^{D-1} [s_n \exp(j2\pi f_\Delta n T_s][(s_{n+D} \exp(j2\pi f_\Delta (n+D) T_s)]^* \\ &= \exp(-j2\pi f_\Delta D T_s) \sum_{n=0}^{D-1} s_n s_{n+D}^* \end{aligned} \tag{3}$$

, where D is the delay sample points between two consecutive training symbols. Therefore, the estimated CFO is obtained from (3)

$$\hat{f}_\Delta = -\frac{1}{2\pi D T_s} \text{angle}(z) = -\frac{1}{2\pi D T_s} \tan^{-1}\left(\frac{\text{Im}(z)}{\text{Re}(z)}\right) \tag{4}$$

The received complex envelope signals of the last two short training symbols perform the autocorrelation operation. The outputs of the real and imaginary parts are used for coarse CFO estimation. After coarse CFO estimation, the fine CFO is estimated by two long training symbols using the same method as the coarse CFO estimation. Under the pipeline circuit structure, the coarse CFO estimation is delayed by 14 clocks to be added to the fine CFO estimation to produce the total CFO estimation for the frequency compensation of the following received data packets signal $r(nT_s)$. The range of

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the CFO estimation is defined as

$$\hat{f}_{range} = \pm\frac{1}{2T} \tag{5}$$

, where T is the training symbol duration.

The CFO estimation and compensation circuits require the evaluation of elementary functions, such as exponential and trigonometric functions, which cannot be supported by FPGA ModelSim's library. In general, a look-up table method adopted to compute the high precision trigonometry function requires a large memory for the FPGA processor. Here the CORDIC algorithm is used to evaluate each of these elementary functions. The CORDIC algorithm, which provides an iterative method of performing vector rotations by arbitrary angles using only shifts and additions, can be operated in either vectoring mode (VM) or rotation mode (RM). In VM, the algorithm computes the length (R) and the angle (θ) towards the x-axis of a vector (a, b).

$$(R,\theta) = (\sqrt{a^2+b^2}, \arctan(\frac{a}{b})) \tag{6}$$

In RM, a vector (a, b) is rotated by an angle (θ) to obtain a new vector (c, d).

$$(c,d) = (a\cos(\theta) - b\sin(\theta), b\cos(\theta) + a\sin(\theta)) \tag{7}$$

The RM CORDIC operation can simultaneously compute the sine and cosine of the input angle (θ) by setting a=1 and b=0 in (7).

$$c = \cos\theta \tag{8}$$

$$d = \sin\theta \tag{9}$$

The exponential of the input angle is extended as

$$e^{-j\theta} = \cos\theta - i\sin\theta \tag{10}$$

The block diagram of the SDR based CFO estimation and compensation circuit is shown in Fig. 1, which can perform the signal processing functions of coarse estimation, long code compensation, fine estimation and CFO compensation by reconfiguring three CORDIC FPGA modules including vectoring module, rotation module and exp_math module. The sequence controller receives the commands from the reconfiguration controller to determine the order of signal processing functions. Different processing functions of the SDR based CFO estimation and compensation circuit can share three common CORDIC FPGA modules operated with different parameters during processing function switching. The parameter change of the command processing modules is trigged by the reset_enable signal. The use of the FPGA is well aligned to the parallel nature of the application functions. The sequence control command is able to download the XILINX FPGA bitstream of an application code stored in the memory to its corresponding modules allocated in each signal processing finction of the SDR based CFO estimation and compensation circuit. The functions of the exp_math module include the exponential function computation, conjugate and multiplication, and accumulation. The vectoring module can process the complex envelope signal to get the estimated CFO frequency. The rotation module can generate the complex envelope signal from the input phase angle. The SDR based CFO estimation and compensation circuit can quickly allocate vectoring module, rotation module or exp_math module to efficiently perform coarse estimation, long code compensation, fine estimation and CFO compensation by mapping the parameter bitstreams onto the same CORDIC FPGA modules according to the processing order presented in Fig. 1. Therefore, different processing functions can reuse the common modules to reduce the hardware cost and power consumption.

III. CORDIC FPGA MODULE CIRCUITS

Due to the FPGA processor adopts binary coding so that tan $(\theta) = \pm 2^{-i}$. The multiplication by the tangent term is reduced to simple shift operation. In RM, the iterative rotation can now be expressed as

$$\begin{cases} x_{i+1} = K_i \cdot \left[x_i - y_i \cdot \delta_i \cdot 2^{-i} \right] \\ y_{i+1} = K_i \cdot \left[y_i + x_i \cdot \delta_i \cdot 2^{-i} \right] \end{cases} \tag{11}$$

, where $K_i = \cos(\tan^{-1} 2^{-i}) = 1/\sqrt{1+2^{-i}}$, $\delta_i = \pm 1$. The product of the K_i's can be treated as part of a system processing gain. The exact gain depends on the number of iterations, and obeys the equation

$$A_n = \prod_n \sqrt{1+2^{-2i}} \tag{12}$$

The angle accumulator is initialized with the desired rotation angle. A rotation decision at each iterative processing is made to diminish the magnitude of the residual angle in the angle accumulator.

$$z_{i+1} = z_i - \delta_i \cdot \tan^{-1}(2^{-i}) \tag{13}$$

, where $\delta_i = -1$ if $z_i < 0$, $\delta_i = +1$ otherwise. The residual angle rate at each iteration is shown in Fig. 2, where initial vector is setting as (1, 0) and angle is changed from-89° to 89° with increment of 1°. The output vector is used to calculate every estimated angle. It indicates the average residual angle rate becomes small when n=14.

In VM, $\delta_i = +1$ if $y_i < 0$, $\delta_i = -1$ otherwise. Then the CORDIC equations are

$$x_n = A_n\sqrt{x_0^2 + y_0^2} \tag{14}$$

$$y_n = 0 \tag{15}$$

$$z_n = z_0 + \tan^{-1}(\frac{y_0}{x_0}) \tag{16}$$

$$A_n = \prod_n \sqrt{1+2^{-2i}} \tag{17}$$

The residual rate of y component at each iterative processing is shown in Fig. 3, where x is setting as 1 and value of y changes from -1 to 1 with increment of 0.01. The output angle is used to calculate every estimated y component. It indicates the average residual rate of y component becomes small when n=14. For the purpose of saving the processing time, the iteration number of the rotation and vectoring

modules is determined as n=14. The vectoring and rotation FPGA modules are a direct translation from the CORDIC equations. The flow charts of the rotation FPGA module and the vectoring FPGA module are shown in Fig. 4 and Fig. 5, respectively.

IV. Experimental Results

Each short training symbol contains 12 subcarriers S. Each long training symbol contains 53 subcarriers L. L and S are input to 64-IFFT to produce 64-QAM-modulated OFDM signals. The duration for each of short training symbols and long training symbols are 1.6μsec and 6.4μsec, respectively. Therefore, using (5), the range of the CFO estimation for short training symbol and long training symbol are calculated as ±312.5 KHz and ±78.125 KHz, respectively. Here the CFO setting $\hat{f}_{\Delta set}$ is 236 KHz and the frequency of the 64-QAM-modulated OFDM test signal is 1985.93 KHz. The CFO estimation and compensation circuit implemented with the CORDIC rotation and vectoring FPGA modules is used to estimate and correct the frequency offset of the input test signal. The performance of the CORDIC CFO FPGA circuit is shown in Fig. 6, where the root mean square error (RMSE) is defined by

$$\mathrm{RMSE} = \sqrt{\frac{\sum_{i=1}^{N} (\hat{f}_{\Delta\_i} - \hat{f}_{\Delta set})^2}{N}} \qquad (18)$$

, where $\hat{f}_{\Delta\_i}$ is the estimated frequency shift at the i_{th} iteration and N is the total number of tests. It shows that the RMSE of the CFO estimation decreases with the increasing E_b/N_0 (dB). The power spectrum density (PSD) of the offset and compensated carrier signals for the 64-QAM-modulated OFDM are illustrated in Fig. 7, where E_b/N_0 = 0dB and the spectrum is spanned in 0MHz~2.5MHz. The frequency shift between the offset and compensated carrier signals is f_Δ = 1985.93 KHz – 1748.82 KHz = 237.11 KHz. The residual CFO is 1.11 KHz, which is less than the tolerable range of 0.01 subcarrier spacing (1.5625 KHz). The residual CFOs with reference to 236 GHz are 0.4979% and 0.4703% for CORDIC CFO FPGA circuit and simulation, respectively. The resource consumption of the CFO circuit implemented in 10 MHz clock FPGA chip is shown in Table I. The FPGA chip has a working cycle of 10 MHz, CFO circuit processing time of (15clocks)/(10MHz)=1.5µsec, satisfying the real time requirements (less than 8µsec) of OFDM transceiver operated with IEEE 802.11p [7] standard.

V. Conclusions

The results of this paper show that the CORDIC FPGA modules can correctly complete the operations associated with CFO estimation and compensation of OFDM transceiver by truncating the iteration numbers to reduce the processing time. In addition, the hardware reconfiguration can save the power consumption and cost of the CFO estimation and compensation circuits. The FPGA clock rate can be increased up to 44.338 MHz to meet the bandwidth requirements of the OFDM systems defined by different standards. Besides, the designed CORDIC rotation and vectoring modules are programmable and reconfigurable so that they are also applicable for future SDR and cognitive radio systems.

Acknowledgment

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References

[1] T. Pollet, M. Moeneclaey, "BER sensitivity of OFDM systems to carrier frequency offset and Wiener phase noise," *IEEE Trans. Commun.*, vol. 43, Apr. 1995, pp191-193.

[2] U. Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, Springer, 2004.

[3] W. Tuttlebee, Software Defined Radio, John Wiley Ltd., 2004.

[4] ModelSim: http://www.model.com/.

[5] Y. H. Hu, "CORDIC-Based VLSI Architectures for Digital Signal Processing," *IEEE Signal Processing Mag.*, vol. 9, no. 3, pp. 16-35, Jul. 1992.

[6] J. Heiskala and J. Terry, OFDM Wireless LANs: A Theoretical and Practical Guide, Sams, 2001

[7] Draft Amendment to Standard for Information Technology – Telecommunications and information exchange requirements – Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specification, IEEE STD 802.11p/D1.0, Feb. 2006.

TABLE I
Resource consumption of CFO estimation and compensation circuit

Circuit Module	Slice Flip Flop (%)	4 input LUTs (%)
CFO estimation	1.76	4.74
CFO compensation	0.09	0.33
Per rotation operation	0.18	1.20
Per vectoring operation	0.15	0.85
Per exp_math operation	0.08	0.73

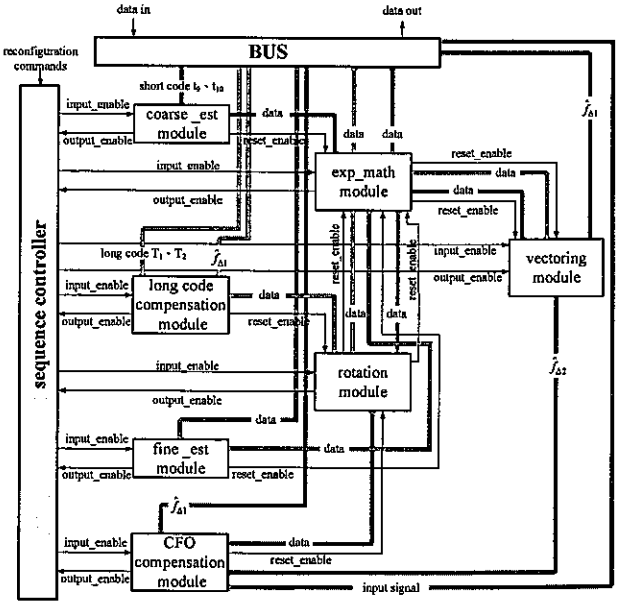

Fig. I Block diagram of the SDR based CFO estimation and compensation circuit

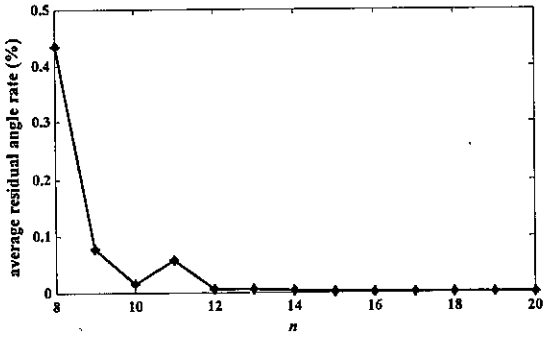

Fig. 2 Decision of the iteration number for rotation module

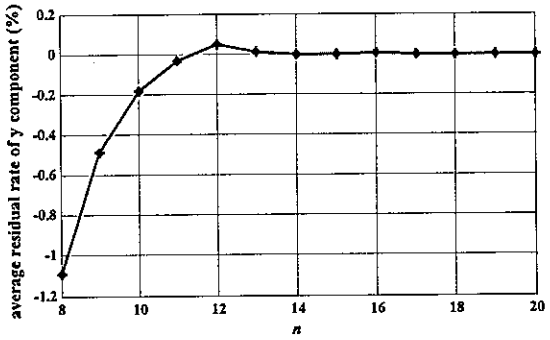

Fig. 3 Decision of the iteration number for vectoring module

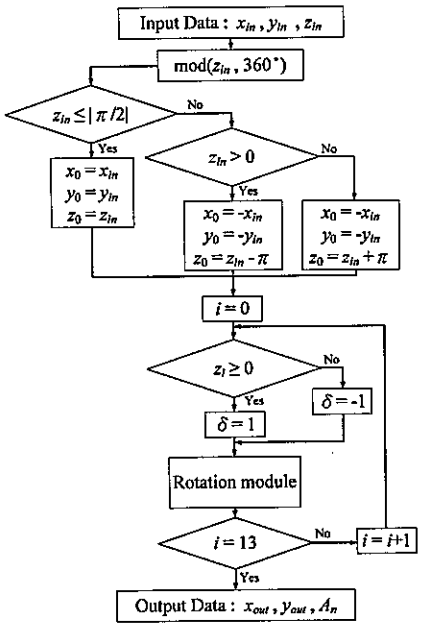

Fig. 4 The flow chart of the rotation FPGA module

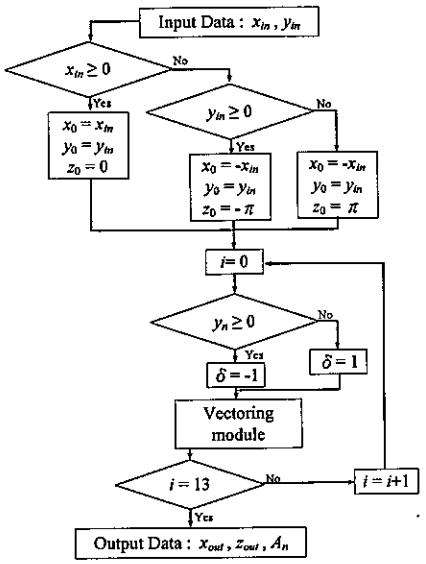

Fig. 5 The flow chart of the vectoring FPGA module

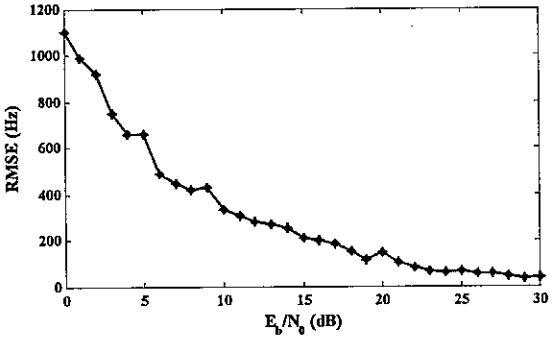

Fig.6 The estimation accuracy of the CFO estimation and compensation circuit

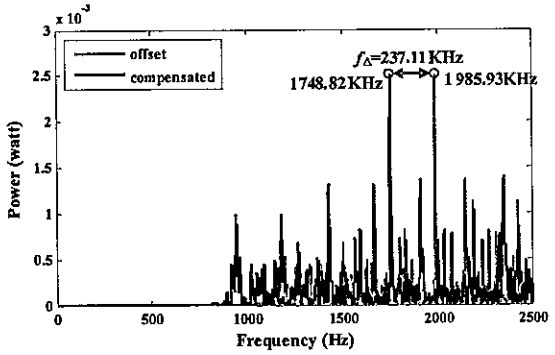

Fig. 7 PSD of the 64-QAM-modulated OFDM output signal of the CFO estimation and compensation circuit