元智大學補助學生出席國際會議報告書

報告人姓名	董慧香	所屬系所	資工所
會議時間地點	April 7-9 2008 Montpellier, France		
會議名稱	IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI (isvlsi2008)		
發表論文題目	Standard Cell Like Via-Configurable Logic Block for Structured ASICs		

報告內容應包括下列各項：

一、參加會議經過

2008 IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI (2008 isvlsi)於法國靠近地中海沿岸的蒙皮立(Montpellier) 城市舉行。4 月 6 日由香港搭乘國泰航空班機抵達法國巴黎機場，再由巴黎機場轉乘法國子彈列車(TGV)到蒙皮立會議地點辦理報到。會議時間總計三天，大會共安排了 2 場專題演講，72 篇論文分為 22 個議程的口頭報告，21 篇海報論文分別在 2 天張貼。我們論文『Standard Cell Like Via-Configurable Logic Block for Structured ASICs』的口頭報告，被安排在 4 月 9 日下午 2:00-3:40 Session 11-A 的第一篇，我的報告過程順利，也在會議餐敘或休息時間，有機會認識來自不同國家的專家學者及學生，實在是一次難得的寶貴經驗，會議於 4 月 9 日圓滿結束後，搭乘 TGV 回到巴黎，13 日由巴黎機場搭機到香港轉機回台灣。

二、與會心得

4 月份能夠出席 2008 isvlsi 會議，由衷感謝指導教授林榮彬老師的殷切指導，所以審稿委員對於我們的論文評價頗高，並且指定為口頭報告的論文，同時也感謝學校研發處補助出席經費，使我可以順利參與會議。在議程中有許多吸引我注意的議題，尤其是有關高速/低功率(high speed/low power)的論文，例如 High Speed Ultra Low Voltage CMOS Inverter 等，因為目前我們在結構化積體電路(Structured ASICs)設計的研究，與標準元件(Standard cell)比較起來，在面積及速度方面的成效相當不錯，未來應該要更周全的考慮到功率消耗的問題。另外， 我也對議程中與 FPGA 的相關研究有興趣，因為我們的研究現在主要是與基本元件庫(Cell-based)的設計方法相比較，未來期望也能加入 FPGA(FPGA-based)設計方法的比較結果，使實驗結果更加完整，也更能突顯研究成效。

對於初次參與國際會議感到相當的雀躍，而且有機會做口頭報告，這對我而言具有相當的挑戰性，指導老師在事前就盡力協助我預備報告內容，這樣的訓練使我在學術的生涯上，向前拓展了一大步。透過參與國際會議可以了解到全世界的專家學者目前的研究趨勢，更有機會可以與研究領域接近的學者有更多的深入討論，從中獲得的意見可以提供未來研究方向調整的參考依據，這對研究生而言是一種很大的激勵。

三、建議

由於一些國際會議常在接近會議時間才通知論文接受結果，所以要申請赴國際研討會的經費補助時間經常很匆促甚至來不及，如果國科會可以將申請時間放寬，對於一些有機會參與的研究生會有很大的幫助。

四、攜回資料名稱及內容

會議論文集光碟資料壹片

五、其他

會議結束後有機會參觀巴黎，見識到這是一個文化與科技整合於一的城市，巴黎地鐵已經百年歷史，地鐵與週邊快速鐵路成為巴黎人非常方便的交通網絡，配合地面上有更多的古蹟建築保存特色完整，成為觀光資源令人印象深刻，惟法國不以英語為國際語言，在法國如進入無法溝通的地方，反觀台灣在這方面確實有優勢，我們早有國際化的遠見，如果可以配合在其他地方更有特色的發展，將來才能在世界佔一席之地。

附件為口頭報告投影片

Standard Cell Like Via-Configurable Logic Block for Structured ASICs

Mei-Chen Li, Hui-Hsiang Tung
Chien-Chung Lai, Rung-Bin Lin

Computer Science and Engineering
Yuan Ze University, Taiwan

Outline

- Introduction
- Existing Via-configurable Logic Blocks (VCLBs)
- Our work
  - Programmable fabric
    - Layout, configurability and composition capability
  - Design methodology
    - Logic packer, placement legalizer
- Experimental results
- Conclusions

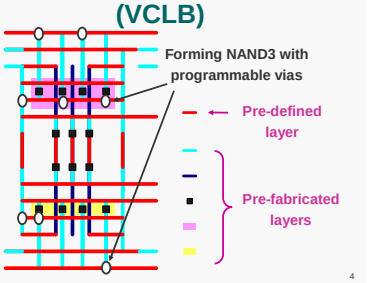
1

Structured ASICs

- Pre-fabricated yet configurable logic blocks (CLB) array with/without a regular routing fabric
- Two programming methods
  - –Via-configurable
  - –Metal-configurable

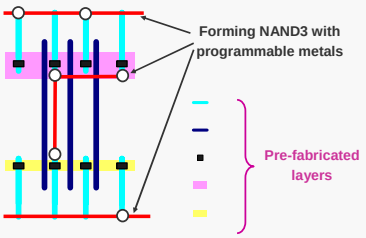
1

Via–configurable Logic Block (VCLB)



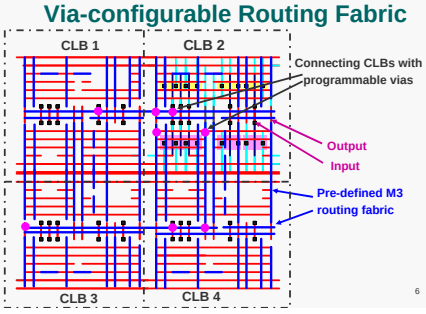
4

Metal-configurable Logic Block



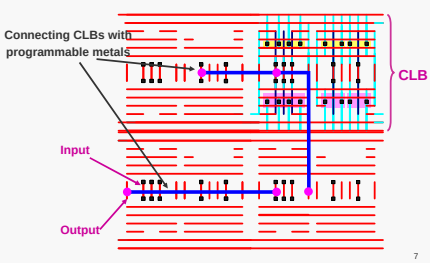
5

Via-configurable Routing Fabric



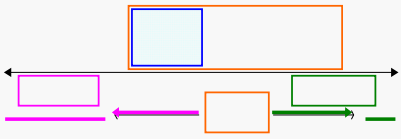
6

Metal-configurable Routing Fabric



7

Programmability Spectrum



8

Programmability Choice

Vendors/ Researchers	Grain size	Programmability		Unified c&s?
		Cell	Routing fabric	
LSI	Fine	Metal	Metal	?
eASIC	Coarse	SRAM-based LUT	Via	No
Virage Logic	Fine	Metal	Metal	?
NEC	Coarse	Metal	Metal	No
AMI	?	Metal	Metal	?
ChipX	?	Metal	Metal	?
Fujitsu	?	Metal	Metal	?
Faraday	?	Metal	Metal	?
Altera	Fine	Metal	Metal	Yes
ViASIC	Coarse	Via	Via	No
Triad Semi.	?	Via	Via	?
Synopsys [5]	Coarse	Via	Via	No
Marek- Sadowska et al.	Coarse	Via	Via	Yes
Pilleggi et al.	Coarse	Via	Metal/Via	No
Ours	Medium	Via	Metal	Yes

9

Design Problems

- CLBs' structure
- Routing fabrics
- Tool support
  - –Cell library development
  - –Placement and routing
  - –Logic synthesis

10

CLB Design Issues

- Basic logic functions realized by a CLB
- CLB composition capability
  - –Form more complex logic functions using more than one CLB
- Transistor utilization of coarse grained CLBs
- Library development efforts

11

Existing VCLBs

- LUT-based [4]
  - Implement *k*-input logic functions
  - Be accompanied by flip-flops for designing sequential circuits
- PLA structure [16]
  - Implement two-level logic functions
  - Be accompanied by flip flops for designing sequential circuits
- Series-parallel layout structure [7]
  - Via-configurable gate array (VCGA)
  - Implement either combinational logic gates or flip-flops
  - *Designing via-configurable logic blocks for regular fabric by* Y. Ran and M. Marek-Sadowska from IEEE Trans. on VLSI Systems 2006

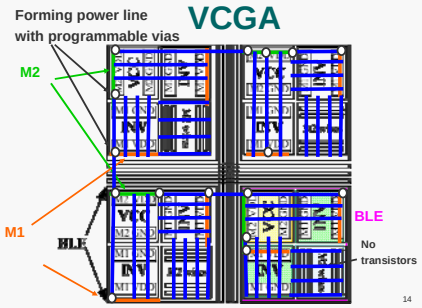
12

VCGA [7]

- 4 Block Logic Elements (BLE)
- 1 VCC + 2 INV in each BLE
- VCC and INV
  - –Via-configurable base-cells with series-parallel structures
  - –VCC: P/G lines on M2
  - –Inverter array (INV): P/G lines on M1

13

VCGA



14

Our work

- Via-programmable CLB (VCLB)
  - Medium grained
  - High composition capability
  - A metal- or a via-programmable routing fabric
  - Implementing combinational or sequential elements
  - Multiple function packed block (MFPB)
  - Placing P/G lines on M2
- Design flow
  - Mostly use commercial standard cell design tools
  - Only develop a logic packer and a placement legalizer

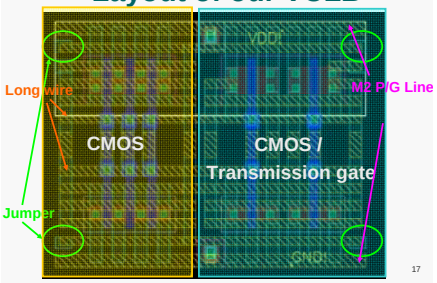
15

Our Standard Cell Like VCLB

- Series-parallel structure
- Major layout features
  - Three diffusion strips for N and P transistors
    - Three pairs of CMOS trans on the left
    - Two pairs of transmission gate trans on the right
  - Power/ground on M2 and located at top and bottom
    - Enabling cell and row abutments
    - Easing power/ground distribution
  - Jumpers on the left and right boundaries to form more complicate logic functions with multi-VCLBs
  - Vias between M1 and M2 for customizing logic function

16

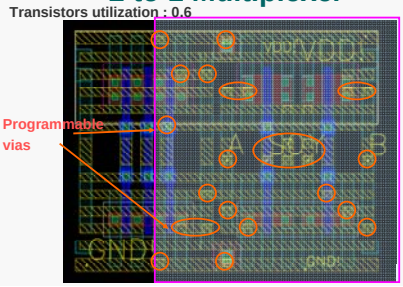
Layout of our VCLB



17

2 to 1 Multiplexer

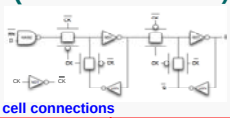
Transistors utilization : 0.6

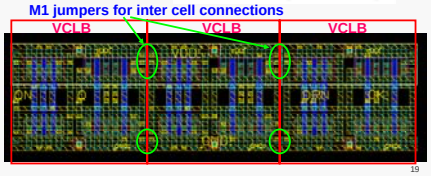


18

D flip-flop (Active Low Reset)

Transistor utilization: 0.73

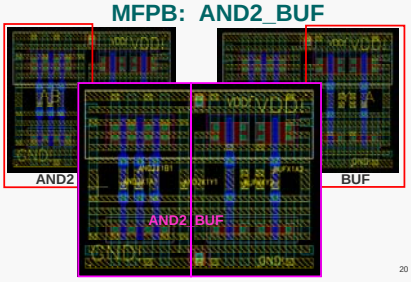




19

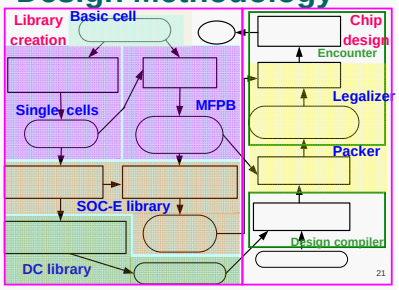
Multiple Function Packed Block

MFPB: AND2_BUF



20

Design Methodology



21

Logic Packer

- Pack two or more cells in a VCLB for reducing cell area and improving the transistor utilization
- Input
  - Circuit netlist from commercial logic synthesizer
- Packing algorithm
  - Model this problems as a graph matching problem
- Output
  - Multiple function packed block (MFPB) netlist

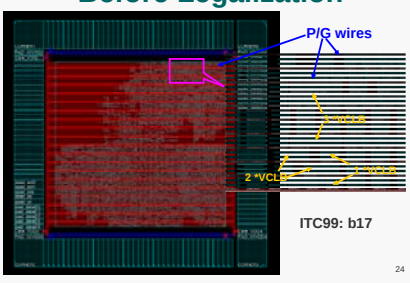
22

Placement Legalizer

- Determine a legal position for each cell such that the total displacement of all cells from their original positions is minimized
  - Legal position must be an integral multiple of VCLB width
- Input
  - Result from a standard cell placer
- Legalizing procedure
  - Create a bipartite graph for each cell row
  - Perform a minimum weight bipartite matching for the cells in each row
- Output
  - Legalized placement

23

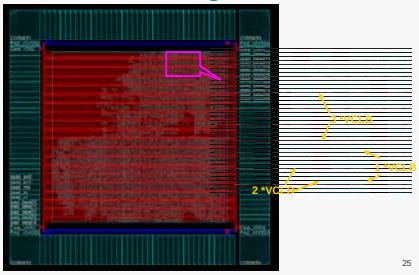
Before Legalization



ITC99: b17

24

After Legalization

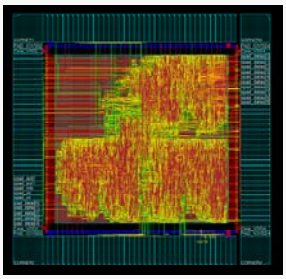


Experimental Results

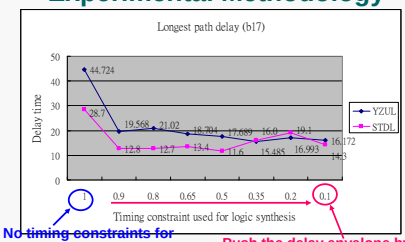
- YZUL (YZU cell library)
  - TSMC 180nm process
  - 78um² for each VCLB area
  - 105 unpacked cells and 73 packed cells
  - Driving capability
    - Logic cell: 1X, 2X,4X
    - Buffer: 1X up to 16X
    - Inverter: 1X up to 20X
    - D flip-flop: 1X, 2X
  - HSPCIE for Power and timing characterization
- Two kinds of experiments
  - YZUL
  - STDL (commercial standard cell library)
- ISCAS and ITC99 benchmarks
  - 11 circuits

Post Routed

ITC99
b17



Experimental Methodology



No timing constraints for minimizing area

Push the delay envelope by synthesizing the circuit with tighter timing

Delay, Power and Area Ratio

		Delay ratio	Area ratio	Power ratio	Delay * power	Delay * area	STDL max/min delay ratio	YZUL max/min delay ratio
ISCAS	s35932	5.8		1	12.2	17.9	6.8	2.8
	s38417	2			4.2	8	1.8	1.3
ITC99	b18	2.9	2.3	1.3	3.6	7.3	3.4	2.2
	b19	1.5	3.7	1.9	2.9	5.7	2.7	2.6
	b20	2.7	1.8	0.6	1.7	4.8	3.4	1.4
	b21	2.8	1.6	0.6	1.7	4.7	3.7	1.8
	b22	4.0	1.9	0.7	2.8	7.5	4.0	1.5
	Ave	**2.7**	**3.0**	**1.5**	**3.9**	**8.0**	**4.4**	**2.5**

The largest longest path delay / The smallest longest path delay

Conclusion and Future Work

- Conclusion
  - Propose a standard cell like VCLB such that existing tools for standard cell designs can be leveraged to design a structured ASIC based on our VCLB
  - Achieve a delay of 2.7 times, an area of 3 times, and a power of 1.5 times that attained by the designs using a commercial standard cell library
- Future work
  - A routing fabric and router

Thank you